unpatentable over U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully traverses the rejections, and requests reconsideration and withdrawal of all rejected claims 1-20.

FINAL Status of Office Action is Premature and Should be Withdrawn

Applicant respectfully requests that the status of FINAL be withdrawn, as it was issued prematurely. In this regard, the presently-outstanding Office Action has changed its basis for rejection for various claims, which were not amended by Applicants' previous response. Therefore, these "new grounds" for rejection were not necessitated by any amendments made to the application. For example, with regard to claim 1, the present Office Action has cited the following additional teachings of Ikeda (the prior art reference relied upon in forming the rejections), which were not cited in the previous Office Action: "Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5 lines 18-56, col. 9, line 45 to col. 10, line 10" and "col. 5, lines 18-56, col. 9, line 54 to col. 10, line 2.")

In responding to the previous Office Action, the undersigned respectfully submitted that the rejections were deficient because the Office Action failed to cite sufficient teachings to the Ikeda reference to support its rejections. Specifically, the undersigned previously noted that general reference to "cols. 2-7" was too general and vague to comply with the requirements of MPEP 707.07 *et seq.* Although the present Office Action did not specifically respond to this allegation, it tacitly agreed by citing additional teachings within the Ikeda patent. This expanded rejection constitute "new grounds" and therefore the presently-outstanding Office Action should have been made non-FINAL.

The present Office Action also changed the rationale for rejecting other claims as well (including the 35 U.S.C. § 101 rejection of claims 15-20).

Summary of Invention

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Rejection of claims 15-20 under 35 U.S.C. § 101

The Office Action rejected claims 15-20 under 35 U.S.C. § 101 because "the claimed computer program ... is directed to a data structure [and] is necessarily to be converted into executable code and executed by a computer to meet statutory requirement." This rejection is just wrong, and is inconsistent with numerous other decisions made by the Patent Office. In

this regard, the Patent Office Action has issued numerous patents with claims directed to "computer-readable mediums" set forth using the same language as Applicant has used for claims 15-20. The following is a list of just a few such patents (each issued on May 28, 2002):

U.S. Patent 6,397,381 (claim 1);
U.S. Patent 6,397,354 (claim 24);
U.S. Patent 6,397,352 (claim 14);
U.S. Patent 6,397,335 (claim 9);
U.S. Patent 6,397,208 (claim 7); and
U.S. Patent 6,397,169 (claim 7).

Therefore, as an administrative agency, which must act consistently from matter to matter and from applicant to applicant, the Patent Office must withdraw this rejection.

Furthermore, and more importantly, the rejection is misplaced and should be withdrawn. In this regard, Applicant respectfully submits that claims 15-20 are NOT directed to a data structure, but rather to "computer-readable mediums." In this regard, claim 15 recites:

> 15. ***A computer-readable medium containing a rules checker computer program***, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

As is clearly recited, the subject matter of claim 15 is directed to a computer-readable medium that "contains" a rules checker computer program. Therefore, claim 15 is properly directed to statutory subject matter (computer-readable media), and the rejection of claims 15-20 (as being directed to data structures) is misplaced and should be withdrawn.

Discussion of Substantive Rejections

Turning now to the substantive rejections of the Office Action, the Office Action rejected all claims as being anticipated by the Ikeda patent.

Fundamental Distinction of the Ikeda Patents

Applicant respectfully traverses the rejections of claim 1-20 of the present application based upon Ikeda, for reasons that will be specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Ikeda and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. The Ikeda patent only mentions the term "noise" in the context of crosstalk noise, and not in the manner taught and treated by the present invention.

In this regard, Ikeda recognizes that a transistor having low output impedance is prone to exert the influence of crosstalk on other wires. However, Ideka also recognizes that a transistor of high output impedance is susceptible to crosstalk from other wires. Accordingly, the system of the Ikeda patent is concerned with crosstalk verification. Furthermore, the system disclosed by Ikeda appears to reference wire patterns and the capacitance measurements therebetween to determine whether crosstalk noise will be problematic.

Discussion of Specific Rejections based upon Ikeda

Turning now to the specific rejections, the Office Action rejected claims 1-20 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully traverses this rejection for at least the reasons that follow.

In rejecting claims 1 and 15, the Office Action states:

> As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as width, length, connected in device channel, etc. (**"Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10**). The program is designed to check **transistor** susceptible **to noise** in the **cross-talk influence** (col. 2, lines 7-24, **col. 5, lines 18-56, col. 9, line 54-col 10, line 2**), including checking noise **susceptible or noise** immunity as claimed **for transistors to other transistors** because they are parts of noise control scheme.

(*Emphasis added* to illustrate the new language added to the present Office Action – the remaining text was present in prior Office Action).

The undersigned has closely reviewed the Ikeda reference and submits that it does not disclose the invention as defined by the independent claims of the present application (now is this analysis changed by the teachings of the newly-cited locations of Ikeda). Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
>
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 1 for at least the reason that Ikeda fails to disclose or teach at least the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of ***crosstalk noise*** as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract).

In contrast, claim 1 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable ***noise immunity***. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Furthermore, the undersigned performed an electronic search of the entire text of the Ikeda patent for the term "noise immunity" and this term is not mentioned anywhere within the Ikeda patent.

The Office Action cited col. 9, line 45 through col. 10, line 10 of Ikeda as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. In fact, this portion of Ikeda teaches the comparison of a width to length ration (W/L) with a stored reference value to identify "the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk." (col. 9, line 68 through col. 10, line 1). In this respect, Ikeda teaches that a transistor with a low output impedance (W/L greater than first reference value) is prone to exert the influence of crosstalk, while a transistor of high output impedance (W/L less than second reference value) is susceptible to crosstalk. Again, and significantly, the assessment of the likelihood of exerting crosstalk or the susceptibility to crosstalk of the Ikeda patent is different than the assessment of noise immunity, as defined by claim 1 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 is misplaced and should be withdrawn. For at least these same reasons, claims 2-7, which depend from claim 1, patently define over Ikeda as well.

Claims 8-14

The Office Action also rejected claims 8-14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Ikeda fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8 stating only:

> As per claim 8, Ikeda anticipated the method for checking design rule including checking transistor design parameters in compatible with different operating conditions or with different transistor layout configuration such that susceptible noise would be checked for high power voltage, heat generation, different transistor threshold, etc. ***According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the crosstalk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54 to col. 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed because they are parts of noise control scheme."***

(*Emphasis added* to illustrate the new language added to the present Office Action – the remaining text was present in prior Office Action).

As can be readily verified from even a cursory review of the cited portions of Ikeda, this cited portion does not disclose a step of "***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity,***" which is specifically claimed in claim 8.

As noted above in connection with claim 1, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of ***crosstalk noise*** as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract).

Like claim 1, claim 8 specifies the analysis of widths of field effect transistors within a gate, to determine whether the gate has an acceptable ***noise immunity***. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Indeed, nowhere does the Ikeda patent even mention the term "noise immunity."

The Office Action cited col. 9, line 45 through col. 10, line 10 of Ikeda as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. In fact, this portion of Ikeda teaches the comparison of a width to length ration (W/L) with a stored reference value to identify "the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk." (col. 9, line 68 through col. 10, line 1). In this respect, Ikeda teaches that a transistor with a low output impedance (W/L greater than first reference value) is prone to exert the influence of crosstalk, while a transistor of high output impedance (W/L less than second reference value) is susceptible to crosstalk. Again, and significantly, the assessment of

the likelihood of exerting crosstalk or the susceptibility to crosstalk of the Ikeda patent is different than the assessment of noise immunity, as defined by claim 1 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 8 is misplaced and should be withdrawn. For at least these same reasons, claims 9-14, which depend from claim 8, patently define over Ikeda as well.

Claims 15-20

The Office Action also rejected claims 15-20 under 35 U.S.C. § 102(e), as being anticipated by U.S. Patent 5,446,674 to Ikeda. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 15 for at least the reason that Ikeda fails to disclose or teach either of the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of crosstalk noise as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract). In contrast, claim 15 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate

has an acceptable noise immunity. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference.

Specifically, claim 15 was rejected on the same grounds as claim 1. For the same reasons advanced above in connection with claim 1 (pertaining to the claim element of analyzing FET widths to determine whether the gate has an acceptable level of noise immunity), claim 15 patently defines over the Ikeda patent.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 15 is misplaced and should be withdrawn. For at least these same reasons, claims 16-20, which depend from claim 15, patently define over Ikeda as well.

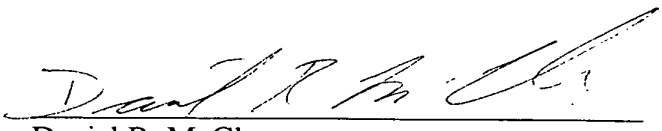
CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 

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